National Taiwan University of Science and Technology

2021 Summer Program

ELEC 220 Digital Logic Circuits

Course Outline

Course Code: ELEC 220

Instructor: Prof. Bevan M. Baas

Home Institution: University of California, Davis

Email: bbaas@ucdavis.edu

Credit: 4

Course Description: Introduction to digital system design including binary numbers and arithmetic, Boolean logic, combinational logic circuit design, design with complex digital gates, latches and flip-flops, clocking and timing, counters, sequential circuits and finite state machine analysis and design

Required Textbooks: *Fundamentals of Logic Design* by C. H. Roth, 7th Edition

Grading & Evaluation:

15% **Homework**

30% **(2) Quizzes**

25% **Midterm exam**

30% **Final exam**

A+:95-100
A:87-94
A-:82-86
B+:78-81
B :75-77

B -:71-74
C+:68-70
C :65-67
C -:61-64
D :55-60

Course Schedule:

Week1

Binary arithmetic

2's complement review

Boolean algebra: basic operators and theorems

Sum of products

Product of sums

Minterms

Maxterms

Incompletely specified functions

Karnaugh maps

Week2

Implicants

Multi-level circuits

NAND, NOR

2-level circuit conversions

Multiplexers

Tri-state drivers

Decoders

Encoders

ROMs

FPGAs

Ripple carry adder

Timing and hazards

Week3

PLDs, PLAs, wired AND/OR

Clockless latches

Level-sensitive latches

Flip-flops

Flip-flop reset and preset

Clocks

Registers

Binary counters, General counters

Intro to Moore & Mealy FSMs

Enable-able registers

Accumulators

Shift registers

Week4

Analysis of Moore FSMs

Analysis of Mealy FSMs

Design of FSMs

Moore binary vs. Mealy binary vs. Mealy One-hot design example

One-hot design

Efficient reset and preset

Moore vs. Mealy critical path

Sequence detection FSM

Critical timing relationships

Adders

Multipliers

Shifters

HDL: Verilog brief introduction